REMARKS

The Applicant appreciates the thorough examination of the present application as evidenced by the Official Action mailed March 24, 2004 (hereinafter "the Official Action"). In particular, the Applicant appreciates the Examiner's indication that Claims 9, 10, 13, 15, 16, and 18-20 would be allowable if rewritten in independent form. In response to the Official Action, the Applicant has rewritten Claims 9 and 10 in independent form thereby placing these claims in a condition indicated allowable in the Official Action. In addition, the title has been amended to correspond to the claims currently pending.

The Applicant has also canceled Claims 1, 6, and 11; rewritten Claims 2, 4, and 7 in independent form; amended Claim 12 to depend from Claim 7; and amended Claim 22 to more clearly define the claimed invention. In the remarks provided below, the Applicant will show that all pending claims are patentable over the cited art. The Applicant thus submits that all claims are in condition for allowance.

Independent Claim 13 And Dependent Claims 14-21 Are In Condition For Allowance

The Official Action states that Claim 13 is "objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." The Applicant notes, however, that Claim 13 is an independent Claim. Accordingly, the Applicant respectfully submits that Claim 13 is allowable in its present form. The Applicant further submits that Claims 14-21 are patentable at least as per the patentability of Claim 13 from which they depend.

Priority Claim

The Official Action states that to obtain the benefit of priority based on priority papers filed in parent Application No. 10/123,601, a claim for such foreign priority must be made in this application. The Official Action further states that in making such a claim, applicant may simply identify the application containing the priority papers.

A certified copy of the priority Korean Patent Application No. 2001-24685 filed May 7, 2001, was previously submitted in U.S. Application Serial No. 10/123,601 (now issued as U.S. Patent No. 6,674,670) from which the present application claims priority as a divisional application. Moreover, the Applicant notes that the cover sheet of the Official Action indicates that: "Certified copies of the priority document have been received in Application No. 10/123,601." Accordingly, the Applicant believes that all requirements for the priority claims to U.S. Application No. 10/123,601 and to Korean Application No. 2001-24685 have been satisfied. If any additional issues relating to the priority claims should need to be addressed, the Applicant respectfully requests that the Examiner contact Scott C. Hatfield (Attorney for the Applicant) at (919) 854-1400. The Applicant appreciates the Examiner's assistance insuring that the priority claims are properly perfected.

All Changes Requested In The Specification Have Been Made

The Official Action requests that Applicant insert the patent number and issue date for U.S. Application No. 10/123,601 in the Related Application section of the specification. In response, the Applicant has amended the Related Application section of the specification to recite the patent number and issue date.

The Official Action further states that Applicant's cooperation is requested in correcting any errors of which the Applicant may become aware in the specification. All errors of which the Applicant is aware have been corrected.

All Claim Objections Have Been Addressed

The Official Action states that in Claim 1, line 1, the word "date" should be --data--. In response, Claims 2 and 4 (which have been amended to include recitations of Claim 1) have been amended to recite "A method of writing data...." Claim 1 has been canceled. The Applicant appreciates the Examiner's assistance in correcting this typographical error.

Claims 2, 3, 7, And 8 Are Patentable Over Ngai

Claims 2 and 7 have been rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 6,400,635 to Ngai et al. (hereinafter "the Ngai patent").

The Applicant respectfully submits, however, that Claims 2 and 7 are patentable for at least the reasons discussed below. Claim 7, for example, recites a memory device comprising:

> a plurality of memory cells wherein each memory cell comprises a latch circuit having first and second complementary latch outputs and first and second write circuits respectively coupled to said first and second latch outputs;
>
> a plurality of write word lines wherein each write word line is coupled with the first and second write circuits of a respective plurality of memory cells;
>
> a plurality of complimentary write bit line pairs wherein write bit lines of each complimentary write bit line pair are respectively coupled with the first and second write circuits of a plurality of memory cells; and
>
> a controller that selects a memory cell to which data is to be written, activates a write word line coupled to the first and second write circuits of the selected memory cell to which data is to be written, and applies complementary write values to complementary write bit lines of a write bit line pair coupled with the first and second write circuits of the selected memory cell, so that the first and second latch outputs of the selected memory cell are coupled with the complementary write bit lines of the write bit line pair coupled therewith to write the complementary write values to the first and second latch outputs of the selected memory cell responsive to activating the write word line coupled to the first and second write circuits of the selected memory cell wherein the controller applies a same value to complementary bit lines of complementary bit line pairs not coupled with the selected memory cell.

Anticipation under section 102 requires that each and every element of the claim is found in a single prior art reference. *W. L. Gore & Associates Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983). Stated another way, all material elements of a claim must be found in one prior art source. *In re Marshall*, 198 U.S.P.Q. 344 (C.C.P.A 1978). "Anticipation under 35 U.S.C. § 102 requires the disclosure in a single piece of prior art of each and every limitation of a claimed invention." *Apple Computer Inc. v. Articulate Systems Inc.* 57 USPQ2d 1057, 1061 (Fed. Cir. 2000). A finding of anticipation further requires that there must be no difference between the claimed invention and the disclosure of the cited reference as viewed by one of ordinary skill in the art. *See Scripps Clinic & Research Foundation v. Genentech Inc.*, 927 F.2d 1565, 1576, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). Additionally, the cited prior art reference must be enabling, thereby placing the allegedly disclosed matter in the possession of the public. *In re Brown*,

329 F.2d 1006, 1011, 141 U.S.P.Q. 245, 249 (C.C.P.A. 1964). Thus, the prior art reference must adequately describe the claimed invention so that a person of ordinary skill in the art could make and use the invention.

In support of the rejection, the Official Action states that: "Ngai et al. disclose the controller (130-2, Fig. 2) applies a same value to complementary bit lines of complementary bit line pairs not coupled with the selected memory cell." The Official Action, however, does not identify any particular portion of the Ngai patent that makes this disclosure. Moreover, the Applicant respectfully submits that the Ngai patent fails to teach or suggest that a controller applies a same value to complementary bit lines of complementary bit line pairs not coupled with the selected memory cell.

Accordingly, the Applicant respectfully submits that Claim 7 is patentable over the cited art. The Applicant further submits that Claim 2 is patentable for reasons similar to those discussed above with respect to Claim 7. In addition, Dependent Claims 3 and 8 are patentable at least as per the patentability of Claims 2 and 7 from which they depend.

Moreover, Dependent Claims 3 and 8 are independently patentable. Claim 8, for example, depends from Claim 7 and thus includes all recitations of Claim 7 as discussed above. In addition, Claim 8 recites that the controller applies a same high logic value to complementary write bit lines of the complementary write bit line pairs not coupled with the selected memory cell. As the Ngai patent fails to teach or suggest applying a same high logic value to complementary write bit lines of complementary bit line pairs, the Applicant respectfully submits that Claims 8 and 3 are independently patentable.

If any rejections based on the Ngai patent should be maintained against any of Claims 2, 3, 7, or 8, the Applicant respectfully requests that the Examiner point out particular portions of the Ngai patent that support the rejection(s).

Claim 4 Is Patentable Over Ngai

The Office Action states that: "Claims 1-5 are rejected as being directed to the method and/or steps derived from the apparatus described in claims 6-8 and 11-14 above." The Applicant submits, however, that the recitations of Claim 4 are not

directed to a method or steps derived from any apparatus described in claims 6-8 or 11-14. If any rejections should be maintained with respect to Claim 4 based on the Ngai patent, the Applicant respectfully requests that the Examiner identify particular portions of the Ngai patent that disclose the recitations of Claim 4, and in particular that disclose:

> generating a control signal on a control line coupled to a plurality of the memory cells; and
>
> responsive to generating the control signal, resetting all of the plurality of the memory cells to a same reset condition.

The Applicant submits that the Ngai patent fails to teach or suggest at least these recitations of Claim 4.

Claim 22 Is Patentable Over Ngai

Claim 22 has been rejected under 35 U.S.C. § 102(a) as being anticipated by the Ngai patent. The Applicant respectfully submits, however, that Claim 22 is patentable for at least the reasons discussed below. Claim 22 recites a semiconductor memory cell including:

> a write word line;
> a write bit line;
> a read word line;
> a read bit line;
> a virtual ground;
>
> a latch circuit for latching a predetermined voltage and including first and second nodes having opposite voltage levels;
>
> a write circuit for transmitting a first external voltage loaded in the write bit line to the first node in response to a signal of the write word line; and
>
> a read circuit for inverting the voltage level of the second node in response to a read signal on the read word line and the virtual ground and transmitting the voltage to the read bit line,
>
> wherein the virtual ground is ground voltage or a supply voltage which can be changed, wherein the virtual ground line is set to a first of the ground voltage or the supply voltage when the read signal is on the read word line and the latch is selected for a read operation and wherein the virtual ground line is set to a second of the ground voltage or the supply voltage when the read signal is on the read word line and the latch is not selected for a read operation.

Ngai does not teach or suggest setting a virtual ground line to a first of a ground voltage or a supply voltage when the latch is selected for a read operation and setting the virtual gound line to a second of the ground voltage or the supply voltage when the latch is not selected for a read operation. In contrast, Ngai states that:

> to read the data out to circuit **150-1**, circuit **140-1** applies a gate-enabling signal to lead **142-1**. This turns on transistor **260-1** in FIG. 3. If the output signal of inverter **230** is also a gate-enabling signal (assumed to be logic 1), transistor **250-1** is also turned on. With both transistors **250-1** and **260-1** on, a short circuit is created between leads **148-1** (normally driven or biased to respective different signal levels or potentials). This short circuit condition is detected by circuit **150-1** as an indication that memory cell **200** is outputting logic 1. If the output signal of inverter **230** is of the opposite polarity (assumed to be logic 0), transistor **250-1** is not turned on, leads **148-1** are not short-circuited to one another, and circuit **150-1** detects this as an indication that memory cell **200** is outputting logic 0.

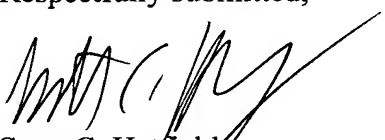
(Ngai, Col. 6, lines 19-33). Neither of the leads **148-1** is the virtual ground line as recited in Claim 22, as the Ngai patent does not teach or suggest either of the leads **148-1** of Ngai being set to a first of the ground voltage or the supply voltage when the latch is selected for a read operation and being set to a second of the ground voltage or the supply voltage when the latch is not selected for a read operation.

Accordingly, the Applicant respectfully submits that the Ngai patent fails to teach or suggest the recitations of Independent Claim 22 and that Claim 22 is thus patentable.

CONCLUSION

Accordingly, the Applicant submits that all pending claims in the present application are in condition for allowance, and allowance of all claims is respectfully requested in due course. The Examiner is encouraged to contact the undersigned attorney by telephone should any additional issues should need to be addressed.

Respectfully submitted,



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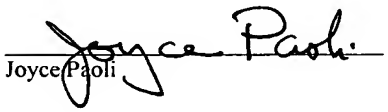

Joyce Paoli